RunX DMA/VDMA IP

AXI4 DMA and video DMA engine for FPGA fabric

IP Core · dma_top

Introduction

The RunX DMA/VDMA IP is a programmable-logic core that moves data between memory and AXI4-Stream interfaces under register control. One RTL tree builds either a descriptor-style DMA engine or a continuous frame-streaming VDMA engine, selected by a single synthesis-time generic, and the two builds present a byte-for-byte identical register map, so one software image drives either bitstream and switching modes on a running board is a bitstream reload with no reboot and no driver change. The RTL uses no vendor primitives. A processor-based system is one common application, and RunX supports that case directly, with ready-made C drivers, a reference design and scripted builds. This brief summarises the core; the datasheet and user guide are the full specification.

Features

- One RTL tree, two build variants: DMA mode and VDMA mode, selected by G_VIDEO_MODE
- Identical register map in both builds; one software image serves either bitstream
- Configurable for up to 32 write and 32 read AXI4-Stream channels, 128-bit data path; 2 + 2 in the delivered build
- Fixed-offset register map with a read-only identification and capability header, so one driver works with any build
- Multi-outstanding AXI4 read and write engines shared by all channels
- VDMA mode: shadowed frame geometry with commit-and-validate, SOF/EOL framing, multi-frame buffering
- Hardware performance counters, so bandwidth is measurable from software without an ILA
- Key-protected soft reset with an AXI quiesce phase and per-stream resets
- Measured on hardware at 97.5 to 99.8 % of the datapath limit, in every direction and at every clock tested
- Vendor-agnostic RTL: no vendor primitive, library or attribute; built unmodified on Vivado, Quartus Pro, Radiant and Libero

IP Facts	
Core Specifics	
Product Name	RunX DMA/VDMA IP
IP Identifier	RUNX-PSPL-DMA-VDMA-v1
IP Version	v1.0
Release Status	Released
Verification Status	Self-checking RTL regression against a golden reference model
Validation Status	Silicon-proven on AMD Kria KV260: both build variants, two Linux driving paths
Provided with Core	
Included	IP · testbenches · C drivers · PL and PS reference design · documentation · technical support
Document	
Document Number	RUNX-PSPL-DMA-VDMA-PB-v2
Document Revision	Rev B
Date	2026-10-06

Synthesis & Implementation

2 write + 2 read lanes · 128-bit · FIFO 1024 · burst 4096

ZU+ xck26 · Cyclone 10 GX · CertusPro-NX · PolarFire

Vendor	LUT	FF	DSP	BRAM
Xilinx	3340 LUT6	2874	0	18
Altera	4439 ALM	4157	0	594 kbit
Lattice	8179 LUT4	3425	0	36 EBR
Microchip	10969 4LUT	4622	0	32 LSRAM

Support

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Introduction

1.1 Overview

The RunX DMA/VDMA IP moves data between memory and AXI4-Stream interfaces under register control. It provides independently configurable read and write stream counts, two of each in the delivered build and regenerable for up to 32, sharing one AXI4 master per direction, all driven through a single AXI4-Lite register interface. The write path is level-triggered into a per-channel circular buffer; the read path is descriptor-style in DMA mode and continuous in VDMA mode.

VDMA mode absorbs frame geometry (line length, line stride, frame size and multi-frame buffering) into the same register map, adding no top-level port. That is what keeps the block design, the address map and the generated device tree identical between the two builds, and what makes mode switching a bitstream reload rather than a rebuild. Everything a driver needs to know about the build it is talking to is readable at run time, so nothing is hardcoded and the wrong driver fails at probe rather than corrupting memory.

The core is fabric logic and assumes nothing about what sits on the other side of its memory interface. A processor-based system is the most common case, and the delivery supports it end to end: a reference design, a Linux kernel module and UIO driver, a portable C HAL and register header, and scripted builds for the AMD toolchain. RunX supports bring-up on other vendors' devices on request.

1.2 Supported Platforms & Toolchains

The RTL is written vendor-agnostic: no vendor library, no vendor primitive, no synthesis attribute, every memory and arithmetic unit inferred. Four independent toolchains build the delivered source with no modification at all, and each build was carried through place-and-route and static timing on a real device of that vendor. The measured maximum frequencies are in section 3.2.

Vendor	Toolchain	Status
AMD / Xilinx	Vivado 2025.2	Built, timed, running on hardware
Altera / Intel	Quartus Pro 25.1	Built and timed
Lattice	Radiant 2025.2	Built and timed
Microchip	Libero 26.1	Built and timed

Core Architecture

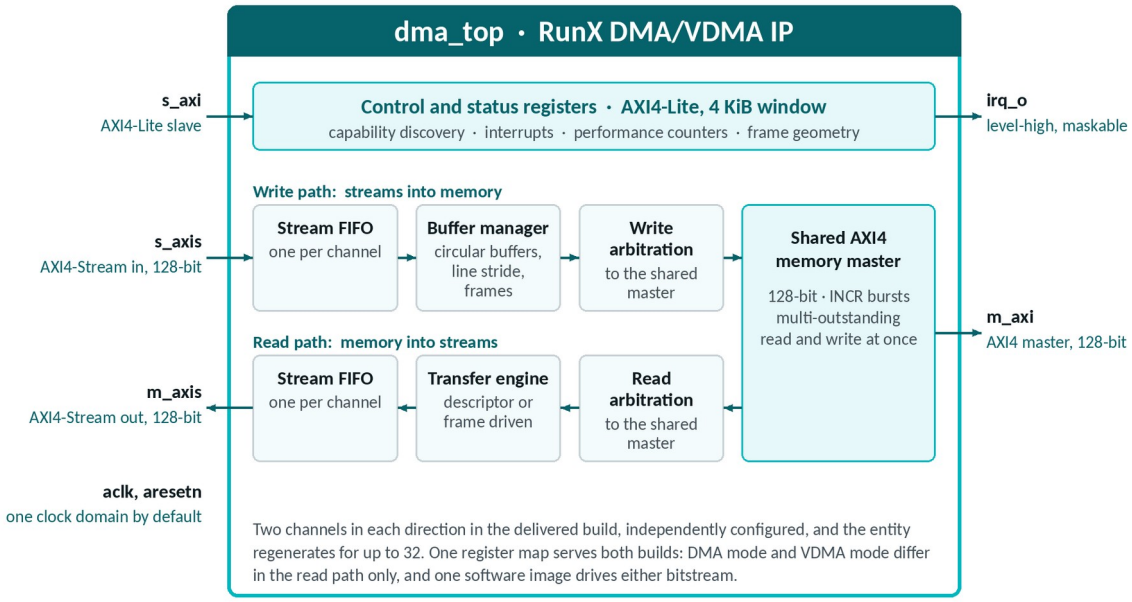


Figure 2-1. The core's own structure, in outline. The datasheet draws it module by module, with the register map and every port.

Performance Summary

3.1 Resource Utilization

Build	LUT	FF	BRAM (tiles)	DSP
DMA, 2 + 2 channels	3340	2874	18	0
VDMA, 2 + 2 channels	3578	3312	18	0
DMA, 8 + 8 channels	7859	5516	72	0
VDMA, 8 + 8 channels	8095	7296	72	0

Out-of-context synthesis of the core alone, Vivado 2024.2, xck26-sfvc784-2LV. Logic grows roughly 850-1000 LUT per added channel pair and block RAM exactly nine tiles: block RAM, not logic, caps the channel count.

3.2 Maximum Frequency (Fmax)

Vendor	Device	DMA	VDMA
Xilinx / AMD	Zynq UltraScale+ xczu7ev-3	335.0 MHz	379.7 MHz
Altera / Intel	Stratix 10 1SG040-1	196.5 MHz	285.4 MHz
Xilinx / AMD	Kintex-7 xc7k70t-1	130.4 MHz	197.5 MHz
Lattice	Avant-E / Avant-X 70-3	117.0 MHz	154.5 MHz

IP-level ceilings for the core alone, measured at the tightest period that met timing; a system built around the core reaches less. Four of eleven measured configurations; the rest are in the datasheet.

Deliverables & Support

The IP with its delivery wrapper; self-checking testbenches and a one-command simulation; clock, reset and interface connection notes; a PL and PS reference design for the AMD Kria KV260; ready-made C drivers; and the documentation set, datasheet, user guide and the field-level register map.

Licensing, pricing, delivery and technical support: info@run-x.com · www.run-x.com